

How Much On-Chip Transient Protection Is Enough?

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July 16, 2012



A lot of marketing hype with regards to on-chip transient protection can be found lately in the datasheets of RS-485 transceivers often used in industrial networking. Claims of up to 15-kV IEC-ESD protection are suggesting that external transient protection schemes are a thing of the past and printed-circuit board (PCB) designs will benefit from eliminating expensive, external transient suppressors.

Unfortunately, this isn't quite true. The amount of transient protection required to maintain the reliable operation of your circuit depends on the application environment in which your circuit must operate and on the type of transients that can be expected within this environment. In fact, heraldic on-chip protection is often insufficient to protect your bus node design against real-world transients.

Major Transient Types

The three major types of transients are electrostatic discharge (ESD), electrical fast transient (EFT), and surge transients. To ensure circuit robustness against these transients, the International Electrotechnical Commission (IEC) has specified a series of transient immunity tests in the IEC61000-4 family of electromagnetic compatibility (EMC) standards: IEC61000-4-2 for ESD immunity, IEC61000-4-4 for EFT immunity, and IEC61000-4-5 for surge immunity.

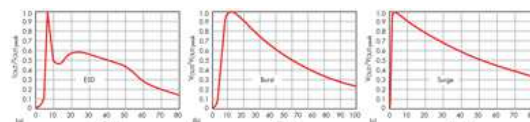
The ESD test simulates the electrostatic discharge of a human onto electronic equipment. Here, an ESD generator generates test pulses with a pulse width of less than 100 ns and a rise time of 1 ns. While this constitutes a pulse of low energy, the high pulse current can destroy a transceiver's internal protection circuitry. Typically a sequence of 20 discharges of positive and negative polarity is applied with a one-second pause between pulses.

The burst test simulates switching transients due to relay contact bounce, or the interruption of inductive loads. These transients often are encountered in industrial environments, such as factory automation and process control.

In this case, a burst generator produces a burst of test pulses. Each burst provides roughly 15,000 transients with rise times of around 5 ns. A test sequence includes six bursts of 10 seconds each with a 10-second pause between bursts. Thus, within one minute several million pulses are applied to the device under test (DUT). Despite the low-pulse energy, the continuous pounding of transients upon the DUT presents an enormous threat to its internal protection circuitry.

The surge test simulates transients resulting from lightning strikes (direct strike or induced voltages and currents due to an indirect strike), or the switching of power systems including load changes and short circuits switching. These transients are about 1000 times longer than ESD or burst transients. Also, the surge generator's low source impedance creates high surge currents at high voltages, producing high-energy pulses.

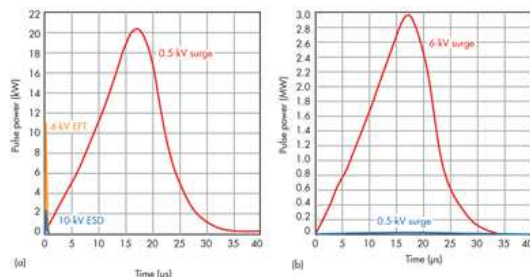
At lower levels (500 V to 1 kV), these transients occur in industrial automation. At higher levels (5 kV to 6 kV), they occur in power grid systems. Because of the high pulse energy, the surge test is commonly limited to five positive and five negative pulses with a one-minute pause between pulses (Fig. 1).



1. The ESD test simulates the ESD of a human onto electronic equipment (a). The burst test simulates switching transients due to relay contact bounce or the interruption of inductive loads (b). The surge test simulates resulting from lightning strikes or the switching of power systems including load changes and short circuits switching (c). Currents and voltages are normalized. For absolute values, refer to the actual standard.

Power And Energy Comparison

To compare the power levels and energy contents between the different transient types unleashed onto a transient protection circuit, test circuits are built and the clamping voltages and currents measured during a transient event. Figure 2 compares the pulse-power of the EFT and surge transients with the power caused by an IEC-ESD transient.

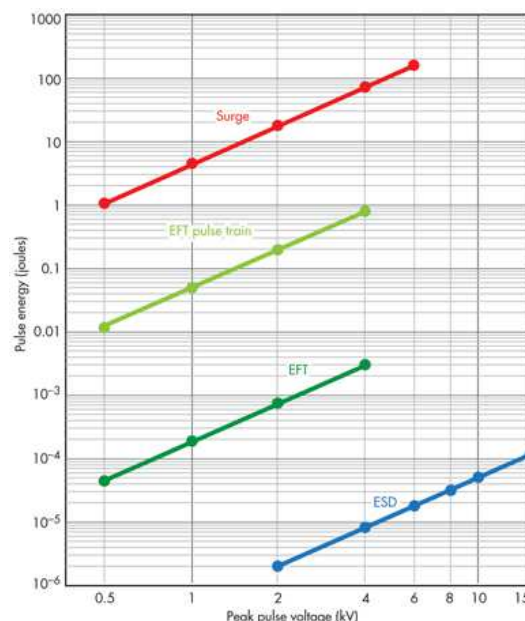


2. There is a significant difference between the pulse power of EFT and surge transients and the power caused by an IEC-ESD transient (a). Then, there's another jump from the power of the 500-V surge transients found in factory environments in industrial and process automation and the 6-kV surge transients in e-metering applications of power grid systems (b).

The tiny blue blip in the bottom left corner of Figure 2a represents the power of a 10-kV ESD transient, which already is dwarfed by the significantly higher EFT power spike and certainly by the 500-V surge transient. This type of transient power is highly representative for factory environments in industrial and process automation.

Figure 2b compares the enormous power of a 6-kV surge transient, which more likely occurs in e-metering applications of power-generating and power-grid systems, with the 500-V surge transient. Note that the pulse-power unit changes from kilowatts to megawatts, pushing the power of the 500-V surge transient almost off the scale.

Figure 3 shows that on-chip IEC-ESD protection can absorb the energy of single ESD and EFT pulses, but it's helpless against the high-energy battering from EFT pulse trains and surge transients, no matter how small the transient voltage is.



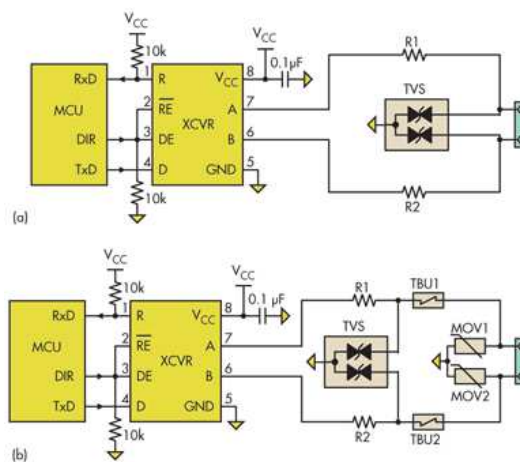
3. On-chip IEC-ESD protection can absorb the energy of single ESD and EFT pulses, but it's helpless against EFT pulse trains and surge transients, no matter how small the transient voltage is.

The constant bombardment of EFTs, also known as pulse train, does not allow the internal protection circuits to recover. The long pulse duration and slowly decreasing pulse power of surge transients signifies high energy content.

The electrical energy of a transient dumped onto the transceiver's internal protection cells is converted into thermal energy, or heat that literally fries the protection cells, destroying the transceiver. Figure 3 showcases the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.

For many novice engineers, it now becomes painfully obvious that even a 15-kV IEC-ESD protection circuit will barely survive a single, 1-kV EFT pulse, let alone a 4-kV EFT pulse train, which has risen to the standard requirement in many industrial automation and e-metering applications.

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary. Figure 4 suggests two circuit designs providing protection against light and heavy surge transients, in addition to ESD and EFT transients. The table presents the associated bill of materials.



4. Different designs can be used to provide protection against light and heavy surge transients and against ESD and EFT transients. Both circuits are designed for 10-kV ESD and 4-kV EFT transient protection. But the circuit (a) provides surge protection of up to 1-kV transients only, while protection circuit (b) can withstand surge transients of 5 kV and more.

Both circuits are designed for 10-kV ESD and 4-kV EFT transient protection. But the circuit in Figure 4a provides surge protection of up to 1-kV transients only, while the protection circuit in Figure 4b can withstand surge transients of 5 kV and more.

Design And Layout Considerations

On-chip IEC-ESD protection is good for laboratory and portable equipment, but insufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node designs require external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. For your PCB design to be successful, start with the protection circuit design in mind.

Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board. Use VCC and ground planes to provide low-inductance paths for the transient currents to return to their source.

Note that high-frequency currents follow the path of least inductance and not the path of least impedance. Design the protection components into the direction of the signal path. Do not force transient currents to divert from the signal path to reach the protection device.

Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC pins of the transceiver, UART, and controller ICs on the board. Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via inductance. Use 1k to 10k pull-up/down resistors to enable lines to limit noise currents in these lines during transient events.

Insert pulse-proof resistors into the A and B bus lines, if the transient voltage suppressor (TVS) clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.

While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs), which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient currents to less than 1 mA.

Conclusion

While implementing IEC-ESD protection on-chip increases the robustness of portable equipment significantly, which most likely experience discharge events due to human contact with connectors and cables, it is insufficient to protect your circuit against EFT and surge transients.

Even if you had a transceiver that survives these high-energy transients, your microcontroller, UART, and voltage regulator most likely won't. What then is the point of receiving data, if no one is home to process them?

References

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Tags: EFT EFT pulse trains electrical fast transient electrostatic discharge ESD industrial control RS485 surges. transient voltage suppression transient protection TVS

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